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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/606,408	06/25/2003	Koji Inoue	544782000200	5662

25226 7590 01/10/2005

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EXAMINER	
SMITH, BRADLEY	
ART UNIT	PAPER NUMBER
2824	

DATE MAILED: 01/10/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/606,408	INOUE ET AL.	
	Examiner	Art Unit	
	Bradley K Smith	2824	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-16* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *12,13 and 16* is/are allowed.

6)☒ Claim(s) *1-11* is/are rejected.

7)☒ Claim(s) *14 and 15* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *25 June 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *6/25/03*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☒ Other: *search notes*.

DETAILED ACTION

Priority

1. Receipt is acknowledged of papers submitted under 35 U.S.C. 119(a)-(d), which papers have been placed of record in the file.

Specification

1. The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed.

The following title is suggested: A memory cell with a perovskite structure varistor.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

3. Claims 1, 2, and 5-7 are rejected under 35 U.S.C. 102(e) as being anticipated by Ueda et al. (US Pregrant Publication 2003/0198077). Uede et al. disclose a variable

resistor and a current controlling device (see figure 42). With regards to claim 2, Ueda disclose a the device is field effect transistor (109). With regards to claim 3, Ueda et al. disclose the use of a diode (see figure 42). With regards to claim 4, Ueda et al. disclose the use of a bipolar transistor. With regards to claims 5-7, Ueda et al. disclose the varistor has a resistance body of a perovskite structure (see embodiment 8).

4. Claims 1 and 4 are rejected under 35 U.S.C. 102(b) as being anticipated by Hasegawa et al. (US Patent 5,038,191). Hasegawa et al. disclose a variable resistor with a bipolar transistor (see claim 11).

5. Claims 1, 3, 10 and 11 are rejected under 35 U.S.C. 102(e) as being anticipated by Lu et al. (US Pregrant Publication 2004/0037106). Uede et al. disclose a variable resistor and a current controlling device (see figure 2). With respect to claim 10 Uede et al. disclose memory cells, each comprising a variable resistor and a diode for controlling a current flowing through said variable resistor; word lines for connecting the anodes of said diodes in common in the row direction of said matrix; and bit lines for connecting one terminal of each of said variable resistors in common in the column direction of said matrix, wherein the cathodes of said diodes are connected to the other terminals of said variable resistors. With respect to claim 11, Ueda et al. disclose the word lines are connected to a row decoder for selecting said word lines, the bit lines are connected to a column decoder for selecting said bit lines, and a readout circuit is connected to said column decoder to read memory data from said memory cells (see figure 2).

6. Claims 8 and 9 are rejected under 35 U.S.C. 102(e) as being anticipated by Inui (US Patent 6,700,813). Inui disclose said memory cells, each comprising a variable resistor and a field-effect transistor for controlling a current flowing through said variable resistor; word lines for connecting the gates of said field-effect transistors in common in the row direction of said matrix; source drive lines for connecting the sources of said field- effect transistors in common in said row direction', and bit lines for connecting one terminal of each of said variable resistors in common in the column direction of said matrix, wherein the drains of said field-effect transistors are connected to the other terminals of said variable resistors (see figure 1). With regards to claim 9, Inui disclose said memory cells, each comprising a variable resistor and a field-effect transistor for controlling a current flowing through said variable resistor; word lines for connecting the gates of said field-effect transistors in common in the row direction of said matrix; source drive lines for connecting the sources of said field- effect transistors in common in said row direction', and bit lines for connecting one terminal of each of said variable resistors in common in the column direction of said matrix, wherein the drains of said field-effect transistors are connected to the other terminals of said variable resistors (see figure 12 and column 2).

Allowable Subject Matter

7. Claims 12, 13 and 16 are allowed.

8. Claims 14 and 15 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

9. The following is a statement of reasons for the indication of allowable subject matter: the prior art of record neither teaches nor suggest the matrix of bipolar transistors with varistors (claims 12, 13 and 16), and the use of perovskite in the memory matrix.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Bradley K Smith whose telephone number is (571) 272-1884. The examiner can normally be reached on 10-6 Monday through Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Richard Elms can be reached on (571) 272-1869. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Brad Smith
Primary Examiner
Art Unit 2824